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EXAMINER

ECKERT II, GEORGE C

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 03192004

Application Number: 08/903,453
Filing Date: July 29, 1997
Appellants: FORBES ET AL.

Robert E. Mates
For Appellant

EXAMINER'S ANSWER

MAILED
MAR 29 2004
GROUP 2800

This is in response to the appeal brief filed December 15, 2003.

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(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: the rejections over Lott et al. are withdrawn. Therefore, the issues presented for review are as described by appellant under issue 6, items I and the first part of IV (brief, pp. 2-3).

(7) *Grouping of Claims*

Appellant's brief includes a statement that claims 2, 3, 24-28, 41-48, 50-52 and 65-68 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Sakata et al., "Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures" Electronics Letters, vol. 30, no. 9, April 28, 1994, pp. 688-89.

Sugita et al., "Floating Gate Transistor and Fabrication Method" Japanese Patent Office, Kokai application 8-255878, October 1, 1996.

Burns et al., "Principles of Electronic Circuits" West Publishing Co., 1987, pp. 382-83.

(10) Grounds of Rejection

The following ground of rejection is applicable to the appealed claims:

Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. in view of Sugita et al. and Burns et al.

With regard to claims 2, 3, 24, 45, 46, 48, 50, 52 and 68, Sakata et al. teach in figure 1 the formation of an insulative layer of amorphous silicon carbide, shown as the a-SiC:H (graded) layer, formed on top of a substrate which is crystalline silicon (c-Si) that can be p-type (see *Sample Preparation*);

a floating gate formed of amorphous silicon, shown as the a-Si:H layer, formed above the amorphous silicon carbide insulator,

a second insulative layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed above the a-Si:H floating gate, and

a control gate shown as metal in figure 1 and later taught as aluminum (see *Sample Preparation*).

And though Sakata et al. teach that the above structure "can be applied to floating-gate memory devices[.]" Sakata et al. do not teach the structure further comprising a source region, a

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drain region, or a channel region there between. However, such regions are taught by Sugita et al. Specifically, Sugita et al. teach, with reference to figure 1, a floating gate memory device comprising:

an N+ type source region 2 and an N+ type drain region 3 (see page 11, para. 0032 of the translated reference which states that the source and drains 2 and 3 are N+ type):

the source and drain regions formed in a p-type silicon substrate (see page 2 of the translated reference which lists the reference numerals and corresponding elements and shows that numeral 1 represents a p-type silicon substrate);

a channel region between the source and drain regions in the substrate (though the channel region is not numbered, it is inherent that there exists a channel region between the source and drain of a transistor, see *Principles of Electronic Circuits*, pp. 382-83 which shows an n+ source and an n+ drain in a p-type substrate and refers to the device as one comprising an “n-channel”);

a floating gate 6 (see page 3 of the translated reference and the list of elements which labels numeral 6 as a polysilicon floating gate) which is formed above and insulated from the substrate;

a control gate 8 formed above the floating gate and separated from the floating gate by a dielectric layer 7 (again, see the list of element on page 3 of Sugita et al. where element 8 is labeled a control gate and element 7 is listed as SiO₂, a known, inherent insulator).

Sakata et al., Sugita et al. and Burns et al. are combinable because they are from the same field of endeavor, which field is the formation of floating gate devices. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a source

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region, drain region and channel region in the device of Sakata et al. The motivation for doing so is that the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack there between, a plurality of floating gate devices can be formed in one substrate and yet be individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art. For example, Burns et al. explicitly teach such programming steps in the paragraph bridging pages 382-83. Furthermore, Sugita et al. generally teach this integration concept in paragraphs 0001-0005 of the translated reference. Therefore, it would have been obvious to combine Sakata et al. with Sugita et al. and Burns et al. to obtain the invention of claims 2, 3, 24-28, 41-48, 50-52 & 65-68.

Regarding the use of polysilicon as the material for the control gate, Sakata et al. indicate that the control gate is formed of aluminum while Sugita et al. are silent as to the material for their control gate. However, Burns et al. teach on page 382 that control gates (or, as labeled there, select gates) are typically formed of polysilicon. Even beyond the teaching of Burns et al., the use of polysilicon as a control gate is considered well known in the art. There are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Sakata et al. from polysilicon.

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is grown on the substrate is

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taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Marosi et al., 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

The rejections of claims 2, 3, 24-28, 41-43, 45-48, 50-52 and 65-68 over Lott et al. in view of Sakata or Lott et al. in view of Sakata and Burns, are hereby withdrawn.

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(11) Response to Argument**I. Introduction**

Appellant begins arguments by citing the MPEP and related court decisions as to establishing a *prima facie* case of obviousness. Specifically, appellant cites MPEP §2143 which lists three criteria needed to show obviousness: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings, 2) there must be a reasonable expectation of success, and 3) the prior art references must teach or suggest all the claim limitations. Appellant cites *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991), which makes clear that the first two criteria must be found in the prior art. Next, appellant cites *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), which requires evidence to support an obviousness rejection and further appellant cites *Dembiczak, Rouffet and Kotzab* (citations omitted) which substantiate the Court's, and thus the Patent office's, need for specificity when making an obviousness rejection. Finally, appellant cites *In re Ratti*, 123 USPQ 349, 352 (CCPA 1959) which requires that a proposed modification made in an obviousness rejection cannot change the principle of operation of the prior art being modified.

Of course, the examiner argues none of the above citations. Rather, it is the above principles that guided the rejections throughout the long history of this application. As should be clear from the above rejection and as will be shown below, the teachings of Sakata, Sugita and Burns, taken together, *clearly* motivate their combination, provide more than a reasonable expectation of success and teach *all* of the instant claim limitations. This was made clear in the

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final rejection as well as the preceding rejections and is supported by a wealth of evidence, which evidence is *replete* in the application's history.

II. Summary of Appellant's Invention

Appellant has summarized the instant invention and provided a representative figure on pages 1-2 of the brief. In sum, the invention comprises a transistor memory device which has typical transistor elements: a source and drain in a substrate with a channel there between (elements 102, 104, 108 and 110), a floating gate and a control gate (elements 106 and 112) where the gates are separated from each other by an insulating layer 114 and the floating gate is separated from the channel by another insulating layer 118. The invention of the instant application lies in the material of layer 118. That layer comprises amorphous carburized silicon (see representative claim 46, brief, p. 5, and specification, page 2, lines 26-27). By using this material, a memory transistor may be programmed using a lower voltage and less time (specification, page 3, lines 5-9). More specifically, the voltage required to induce electrons to tunnel across this material and onto the floating gate is lower in comparison to the voltage required to cause electrons to tunnel across silicon dioxide, which is the typical material used in the art (specification, page 1, lines 20-24; see also Burns, p. 382, figure 9.10(b) using silicon dioxide insulator, SiO₂).

III. Background Considerations of The Technology

In any floating gate memory device, the floating gate may be either programmed such that electrons are placed on the floating gate or not programmed, such that the electrons are removed from the floating gate (*see* Burns, pages 382-83, noting fig. 9.11). When the device is not programmed, application of a threshold voltage to the control gate via the word line will

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cause enhancement of the channel region and allow conduction between the *source* and the *drain*. As Burns explains on page 382 and shows in figure 9.10(a), this conduction is ultimately between the bit line and ground via the drain and source regions respectively. Connecting the bit line to ground by means of the source and drain regions represents a binary '1' as is explained by Burns and shown in figure 9.11(a). Conversely, when the device is programmed and electrons are stored on the floating gate, those electrons raise the "on" voltage of the device such that application of a threshold voltage to the control gate will not cause enhancement of the channel region and conduction cannot occur between the source and drain. This state represents a binary '0' and is shown in figure 9.11(b).

The source and drain regions also serve another fundamental purpose in a floating gate memory device. As explained by Burns on page 383, it is the source and drain regions that provide the electrons for storage on the floating gate. By providing each floating gate device with its own source and drain regions, each memory cell can be individually programmed using "address circuitry." *Burns, p. 383*. The address circuitry applies specified voltages on the source and drain regions, thus making electrons available for programming the floating gate.

The ability to selectively program a memory cell and thus choose an output of binary '1' or '0' allows the transistor to serve as a memory device. As shown above, *this memory function absolutely depends on and is only achieved by the inclusion of source and drain regions*. There is nothing inventive in this manner of operation; it is fundamental to a floating gate memory device and is well known in the art. It is taught by any of Burns, Ng and Wolf, all of which were either used in the rejection or cited during prosecution as evidence (see Paper No. 35, pages 10-12).

IV. Summary of the Rejection Over Sakata In View of Sugita and Burns

The final rejection was made using Sakata as the primary reference. Sakata teaches a memory device as shown by the band diagrams of figure 1, best seen in the “zero bias” diagram on the right side of the figure. Specifically, Sakata teaches a crystalline silicon substrate (c-Si) on which is formed *an insulating layer of amorphous carburized silicon* (a-SiC:H), a floating gate of amorphous silicon (a-Si:H), a second insulating layer of amorphous carburized silicon (a-SiC:H) and finally a control gate of metal. In short, Sakata teaches the instant claim but for the inclusion of a source and drain with a channel there between. See also appellant’s description of Sakata on page 6 of the brief, which comports with the above.

Because Sakata did not expressly teach source and drain regions or a channel there between, Sugita and Burns were cited for these elements. On pages 2-3 of the translated copy, Sugita teaches a floating gate transistor comprising a silicon substrate 1, a twin insulating layer comprising silicon dioxide 4 and carburized silicon 5 above the substrate, a floating gate 6 above the insulator, a second insulating layer 7 above the floating gate, a control gate 8 and finally the necessary source and drain regions 2/3. Of note, Sugita uses a carburized silicon layer 5 as an insulator between the floating gate and substrate. Burns was cited because it teaches that a channel region is inherent between a source and drain of a transistor, such as the transistor taught by Sugita and for teaching the fundamental nature of a floating gate device.

Motivation for combining the references was clearly established in the final rejection and supported with evidence throughout the history of the application. First, in the body of the final rejection as seen on page 5 (paper No. 44), motivation was established by stating that the inclusion of source and drain regions in Sakata would allow an array of floating gate devices to

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be formed in the same substrate and yet be individually written and erased. The formation of an *array* of floating gate devices, each having sources and drains, allows a plurality of binary data to be stored in a single device. As discussed above, this function is well known in the art and specifically taught by Burns; it is the flow or no-flow of current between the source and drain that allows recognition of a binary '1' or '0.'

Second, this knowledge regarding the need for source and drain regions in a floating gate memory device was substantiated earlier in the prosecution history and the additional references remain applicable here. In a previous final rejection (paper No. 35) the instant claims were identically rejected over Sakata, Sugita and Burns. Appellant had cited the then recent case of *In re Lee* and raised an argument that there was no evidence that supported the cited motivation. In response to that argument, the paragraph bridging pages 13-14 of the previous rejection included *seven* additional references that taught that a floating gate device needs sources and drains so that the individual devices may be formed in an array. These references include two textbooks (Burns and Ng), four US patents to others (5,623,442, 5,912,837, 6,144,581, 5,317,535), and one US patent to applicant (5,740,104).

Third and perhaps most importantly, the final rejection (and at least all rejections since paper no. 35) also clearly points out the explicit suggestion to combine as stated in the last full paragraph of the first column of Sakata:

In this Letter we propose and experimentally confirm that the HJ structure shown in Fig. 1 can be applied to *floating-gate memory devices*." (Emphasis added).

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It is hard to imagine a more strait forward manner of suggesting that Sakata be combined with Sugita and Burns to include source and drain regions, which regions are necessary in a floating gate memory device as discussed above.

In sum, the final rejection clearly satisfied the three required elements for establishing a *prima facie* case of obviousness. First, motivation *and* suggestion to combine the references were found in the references themselves and from knowledge generally available to one of skill in the art, which was all made of record. Second, there was a reasonable expectation of success based on the wealth of knowledge in the art as cited, that the addition of source and drain regions to Sakata would allow its application in an array of floating gate devices. And third, the references when combined taught *all* the limitations of the instant claims.

V. Response to Appellant's Specific Arguments

As a preliminary matter, appellant refers in several places to Sakata's device as a "HJ diode structure." *Brief, pages 5-8, emphasis added.* This is a misnomer attempting to draw a distinction where there is none. Sakata does use the term "diode" at least four times in the disclosure but in every occurrence modifies the term as either a "test diode" or a "sample diode."

The best example of the term "diode" used in context comes from Sakata's abstract:

It has been proposed and experimentally confirmed that band-engineered hydrogenated amorphous silicon (a-Si:H)/hydrogenated amorphous silicon carbide (a-SiC:H) heterojunctions on c-Si **can be applied to electrically programmable and erasable memory devices.** A **test diode** with the structure c-Si/graded a-SiC:H/a-Si:H/uniform a-SiC:H/Al exhibits a large hysteresis in the C-V characteristic with a retention time of 0.8s at room temperature. (Emphasis added).

It is clear that Sakata has not taught a conventional diode device but instead is simply referring to a test structure as a diode. Indeed, as highlighted in the above citation, Sakata uses the "test

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diode” to show its application in an electrically programmable and erasable memory device - a floating gate device. This is confirmed by Sakata’s own statement that the device “can be applied to floating-gate memory devices.”

**A. Any Differences In Operation Between Sakata And Sugita
Are of No Moment to the Instant Rejections**

Appellant’s primary concern and thus first argument with the final rejection is that “there are substantial differences between the principles of operation of the HJ diode structure of Sakata and the principles of operation of the floating gate transistor of Sugita.” *Brief*, p. 7. Based on these differences, appellant argues there is no reasonable expectation of success and thus the rejection must fail. *Id.* However, as will be shown below, these arguments are not persuasive. The operating principles pointed out by appellant are of no moment to the instant rejection and certainly do not undermine the reasonable expectation of success.

Appellant quotes Sakata, which teaches the use of electrons *and* holes respectively during the write and erase mode of its device. *Brief*, pp. 7-8. Appellant next compares Sakata to Burns. Burns, like Sakata, writes to a floating gate with electrons *but*, unlike Sakata, teaches an erase mechanism using UV light and does not mention using holes. *Brief*, p. 8. Based on these differences, appellant states that “adding elements from Sugita to the HJ diode structure of Sakata would require a change in the basic principles under which the Sakata construction was designed to operate” and therefore the rejection must fail. *Id.* This argument misapprehends the teachings of Sakata and Burns and is not persuasive.

First, it is not dispositive that Burns does not mention holes in the erase process of a floating gate device, especially in light of the teaching of Wolf (of record, cited in paper No. 35). Specifically, Wolf, on pages 625-26 explains the program and erase mechanisms of a floating

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gate device. There, Wolf teaches that floating gate devices, like the devices of Sakata, Sugita and Burns, are programmed by storing electrons on the floating gate. The storage electrons are obtained by the creation of hot electrons near the drain which electrons traverse the oxide (gate insulator) and charge the floating gate. Wolf also teaches that to erase the cell, as in the teaching of Burns, UV light is applied to the gate. However, unlike Burns which only states that the UV light imparts energy to the electrons which allows them to escape, Wolf gives a better explanation of the mechanism. Specifically, Wolf teaches that "the UV light creates electron-hole pairs in the SiO₂, providing a discharge path for the charged floating gate." As such, holes are involved in the erase process of a floating gate device.

Furthermore, by forming the floating gate between a source and drain, voltage may be applied to selected sources and drains to program or erase an individual cell. It is the source and drain regions that provide the electrons that are either stored or erased from the floating gate, regardless of *how* they are stored or erased. The use of source and drain regions as suppliers of electrons is well known in the art; it is taught by Burns, by Ng and by Wolf. For example, Burns teaches on page 383 that an individual cell is programmed by application of voltage to form a channel region between a source and drain, and from that channel region, electrons are excited and gain enough energy to charge the floating gate. Note the similarity between this description in Burns with that of Sakata - electrons are injected from the substrate into the floating gate.

But even more important, regardless of the mechanism of charge storage or erasure, the combination of the references does *not* change the principle of operation of either device and thus does not negate their combination. That is, Sugita was relied on merely for teaching the use of source, drain and channel regions. The addition of these regions in the device of Sakata will

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not alter the manner in which electrons are stored on or erased from the floating gate. Sakata teaches that the device is programmed and erased by application of specific voltage to the control gate. This method would not be altered by the addition of source and drain regions in the substrate. Rather, as made clear in the rejection, the use of source, drain and channel regions simply facilitates using Sakata's HJ structure in an array. In all, the argument is not persuasive.

B. Sakata's Use of C-V Characteristics to Show the Features of the Device Does Not Undermine Its use in a Floating Gate Memory Structure

Appellant makes a brief argument on pages 8-9 regarding Sakata's figure 2. In figure 2, Sakata shows the capacitance-voltage (C-V) characteristics as exhibited by the sample test device, which C-V curve shows a hysteresis or memory function. Appellant has supplied a paper by Qian that also shows a C-V plot. Qian measures the storage time of holes in a capacitor structure. Based on this similarity (that both Qian and Sakata show a C-V plot), appellant concludes that the device of Sakata may only be used in a DRAM device as opposed to a floating gate device. This conclusion cannot stand.

First, Sakata states, in no uncertain terms, that the structure may be applied to floating gate memory devices. Appellant acknowledges Sakata's statement but summarily dismisses it, noting that it "does not comprise a clear and particular teaching or motivation to one skilled in the art at the time the invention was made to form a device by combining elements from Sakata, Sugita and Burns, and in fact the whole of the text of Sakata teaches away from such a combination." *Brief*, p. 9. It is not understood how Sakata's plain statement is anything *but* a clear and particular motivation to form Sakata's structure having a source and drain as taught by Sugita and Burns.

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Secondly, that Sakata shows C-V characteristics of the test structure supports rather than undermines its use in a floating gate device. A floating gate, by definition, is made of an electrically conductive material that is electrically isolated from all other elements; in other words it is "floating." The substrate of the device is also conductive and is isolated from the floating gate by an insulator, in this case amorphous carburized silicon. This structure, of floating gate-insulator-substrate, is nothing more than a simple capacitor; two plates with a dielectric in between. The C-V plot of Sakata's figure 2 is simply showing the capacitance between the floating gate and the substrate. Its purpose is to show that after electrons are placed on the floating gate and the programming voltage is removed, the electrons remain on the floating gate; hence the hysteresis, and therefore memory function of the device. This explanation here is merely a summary of that taught by Sakata on page 688, second column under *Results and Discussion*. In all, appellant's argument that the C-V plot undermines the rejection based on comparison to Qian is not persuasive.

C. Comparison of Sakata's Invention to Capasso's Does Not Undermine the Instant Rejection

As argued by appellant, Sakata compares its structure to one constructed by Capasso, stating that "Capasso reported similar memory devices based on AlGaAs/GaAs HJ." *Sakata*, column 2. Sakata makes the comparison to point out that Sakata's structure does not suffer from excessive leakage current as did Capasso's. *Id.* From this comparison, appellant makes the argument that Sakata must operate like Capasso and therefore cannot be combined with Sugita and Burns. This argument is without merit.

Attention was first drawn to Capasso by the examiner in paper No. 35. On page 14 of that paper, in further response to appellant's continuing arguments that Sakata could not be

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formed with sources and drains, the examiner pointed out that Sakata itself stated it was similar to the device of Capasso and that Capasso taught the use of sources and drains. Now, appellant argues that because Capasso operates differently from Sugita, and because Sakata says it is similar to Capasso, Sakata cannot be combined with Sugita and the rejection must fail.

Appellant points out that Capasso injects electrons into the floating gate from the control gate. This is different from that taught by Burns and Sugita who inject electrons into the floating gate from the substrate/channel. As such, appellant argues that, because Sakata says it is similar to Capasso, Sakata too must inject electrons into the floating gate from the control gate and thus it cannot be combined with Sugita. *Brief, p. 10*. This directly contradicts the clear teaching of Sakata, as quoted by appellant; “electrons ... are efficiently injected *from the crystalline Si (c-Si) substrate*” (*Sakata, col. 1, Brief, p. 7, emphasis added*). As such, Sakata does *not* operate like Capasso. But, even if it did, such operation would not undermine the combination of Sakata with Sugita and Burns. The electron storage operation of Sakata is not altered in any means by the addition of a source and drain. This was explained above in detail. In all, the argument by comparison to Capasso is without merit and not persuasive.

D. Comparison of Sakata’s Invention to Lott-1 Does Not Undermine the Instant Rejection

Similar to the argument made immediately above, appellant now argues that Lott-1, a reference at best only tangentially related to the entire issue, undermines the rejection based on the structure it teaches. Appellant argues that because Lott-1 refers to Capasso, and Sakata refers to Capasso, Sakata’s final structure using sources and drains would look like Lott-1. *Brief, pp. 10-12*. Therefore, if source and drain regions *were* formed in the device of Sakata, they must be

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formed *next to* the floating gate and not in the substrate as instantly claimed. This argument is also without merit.

First, it is noted that appellant now seems to concede that Sakata does intend its structure to be used as a floating gate memory device. *Brief, p. 11*. However, appellant's conclusion of similarity and thus application of Lott-1's structure, all by way of reference in Lott and Sakata to Capasso, onto the device of Sakata is simply too much. The only similarity between the three references is that they teach floating gate memory devices, *all using sources and drains*. However, Lott-1, like Capasso, forms its device in an AlGaAs based substrate. Sakata, like Sugita, Burns, Ng, Wolf, and the many other references cited in the prosecution, forms its device in Silicon. And as is *taught* by Sugita, Burns, etc., a floating gate device formed in silicon has its source and drain formed in the substrate. Conversely, there is no suggestion, *anywhere* that the silicon-based device of Sakata would, or even could, form a source and drain next to the floating gate as shown in Lott-1's AlGaAs device. Rather, Sugita and Burns each provide an explicit teaching that the source and drain should be and easily could be formed in the *substrate* of Sakata. In all the argument is not persuasive.

E. The Final Office Action And the Prosecution History Is Replete With Evidence Supporting the Addition of a Source and Drain Region in the Device of Sakata.

Appellant's final argument on pages 12-13 of the brief is made against the motivation used in the final rejection. As stated above and pointed out by appellant, the motivation for modifying the device of Sakata by adding a source and drain region is that those regions "allow individual floating gate devices to be formed in an array. ... [t]he use of the source/drain/channel regions for such programming is well known in the art." *Brief, p. 12*. Appellant here argues that

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“the office action did not cite evidence in the record, such as one of the references, that supports the above-stated motivation for combining Sakata, Sugita and Burns as is required by *In re Lee*.”

Id. This argument is not persuasive as it simply ignores the many references, used in the rejection and cited during prosecution, that support the motivation.

As discussed above in the *Summary of Rejection* section (*supra*, pp. 10-12), there were *seven* additional references cited as evidence in support of the motivation. But even beyond this *additional* evidence, the cited motivation has sufficient evidence in the teaching of Burns as used *in the rejection itself*. Burns clearly teaches that the source/drain regions are used to provide electrons for programming a floating gate device. Burns also teaches that the source/drain regions allow forming the floating gate device in an array such that many individual bits may be formed together to achieve the kilobyte memories that were known (e.g. the 256k Intel chip as discussed by Burns, p. 383). None of this information is new as it is simply a reiteration of Paper No. 35, pages 13-14. In all, there is simply no support for appellant to now say that the rejection lacks supporting evidence. The evidence was provided, was discussed at length, and has not been shown in error.

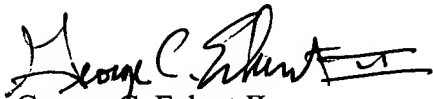
Lastly, appellant makes a brief argument as to the use of polysilicon in place of aluminum as the control gate, stating that no evidence was provided that supports the proposition of using polysilicon as a control gate. This argument simply ignores what is taught by Burns. Burns clearly teaches the use of polysilicon as a control gate on page 382. This was discussed in the final rejection as repeated above. As is known in the art, polysilicon may be doped to a low resistivity and is able to withstand higher temperatures than aluminum. This motivation for its use was stated in the final rejection. Beyond that, it is a simple material substitution, well known

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in the art as clearly taught by Burns, to use polysilicon as a control gate. Arguing now that the use of polysilicon in place of aluminum is not supported by evidence simply ignores that which is well known in the art and explicitly taught by Burns. It is not persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



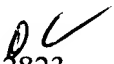
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